

REMARKS

Specification

The specification has been amended as suggested by the examiner to overcome the objection.

Claim Rejections – 35 USC § 102

Claims 1 - 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Conner (US 5,794,175). Applicant traverses this rejection.

Claim 1 recites a control unit configured to electrically connect a corresponding driver and comparator unit to a pin of the semiconductor device under test, or DUT. Conner does not disclose electrically connecting a corresponding driver and comparator unit to a pin of the DUT. Instead, Conner discloses only electrically connecting a whole memory device to a driver/comparator unit. See, for example, Figure 3A of Conner. Claim 1 is therefore not anticipated by Conner. For at least these reasons, claims 2 – 7, which recite additional novel and non-obvious features, are also in condition for allowance.

Moreover, claims 2 and 3 recite a control unit, which can be a multiplexer, that electrically connects a driver/comparator unit to a single pin. Claims 2 and 3 are also not anticipated by Conner because multiplexer 336 only selects among columns of memory devices and not individual pins of a semiconductor device as in Park claims 2 and 3. Specifically, in Figure 3A of Conner, SEL line controls the multiplexer 336 which determines which column of memory devices is to be electrically connected to the driver/comparator unit via the memory devices' output enable. This configuration cannot choose individual pins for electrical connections to the driver/comparator unit, but only whole memory devices.

Claim 8 recites electrically connecting a comparator and driver unit to a pin of the semiconductor device, or DUT. Conner does not disclose electrically connecting a comparator and driver unit to a pin of the DUT. Instead Conner discloses only electrically connecting a whole memory device to a driver/comparator unit. See, for example, Figure 3A of Conner. Claim 8 is therefore not anticipated by Conner. For at least this reason, claims 9 – 11, which recite additional novel and non-obvious features, are also in condition for allowance.

Claim 12 recites a pattern memory comprising an input pattern memory and an output pattern memory. For example, as shown in the embodiment of Figure 2, and discussed on page 5, the applicants' output patterns and input patterns are stored in the pattern memory

324, allowing the semiconductor device test system to be stand-alone and independent of a work station. Conner does not disclose a memory for output patterns nor input patterns. In Conner, the work station 110 is depended on to convey output patterns and input patterns that test the semiconductor memory devices. See, for example, Figures 1 and 2. Claim 12 is therefore not anticipated by Conner. For at least this reason, claims 13 – 15, which recite additional novel and non-obvious features, are also in condition for allowance.

Claim 16 recites selectively connecting a pin of the test system to a pin of the semiconductor device, or DUT. Conner does not disclose connecting a pin of the test system to a pin of the semiconductor device, or DUT. Instead Conner discloses only connecting a whole memory device to a driver/comparator unit. See, for example, Figure 3A of Conner. Claim 16 is therefore not anticipated by Conner. For at least this reason, claims 17 – 20, which recite additional novel and non-obvious features, are also in condition for allowance.

Applicant requests reconsideration in view of the foregoing amendments and remarks. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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